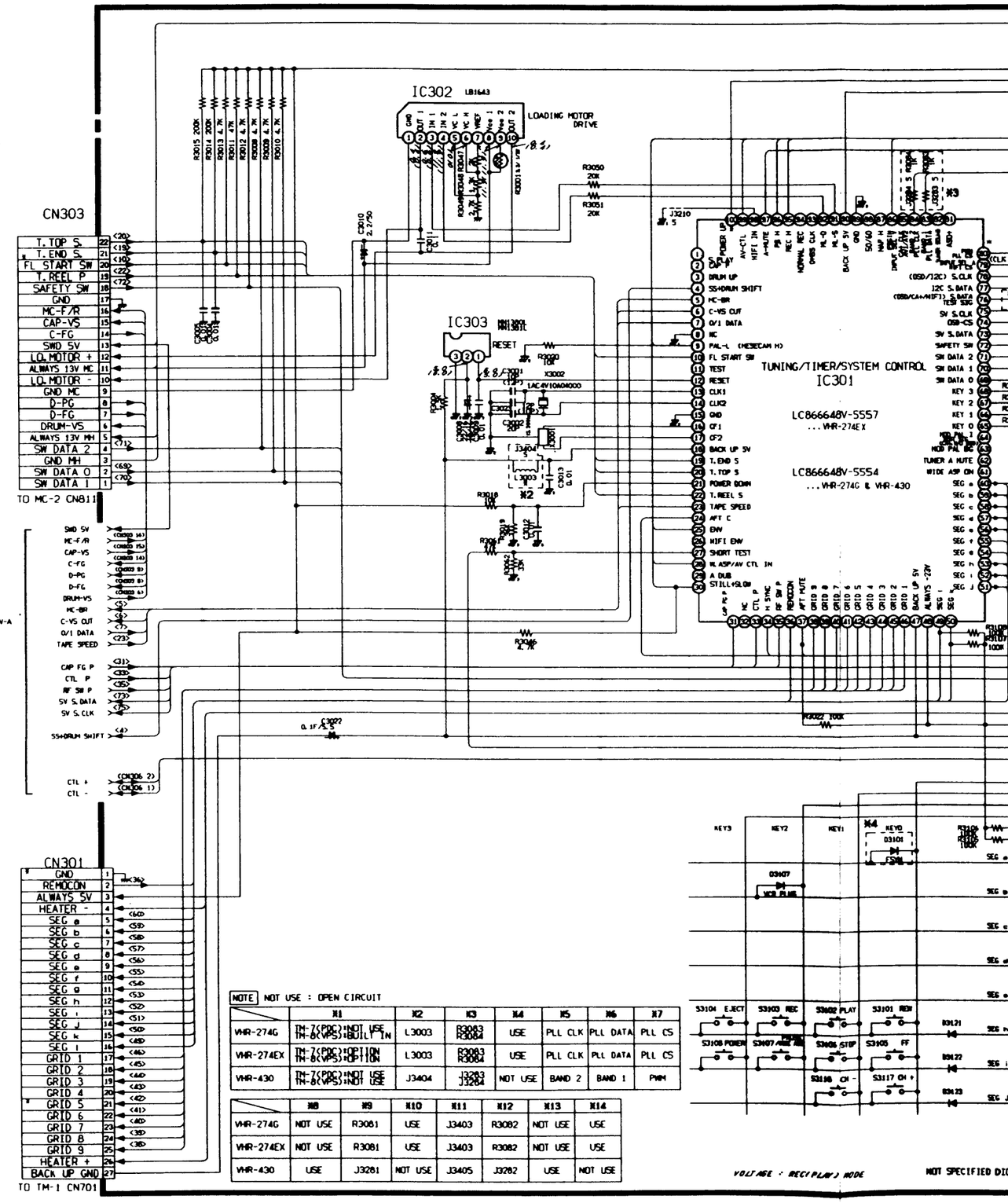
IC301 SYSTEM CONTROL,TIMER, & TUNING CONTROL MPU PIN FUNCTIONS TABLE

No.	Name	I/O	I/O Signal Function
1	S - PLAY	O	Signal for indicating CUE , REV , STILL and SLOW modes.
2	CAP P.	O	Gain down control for Head Motor Amplifier at SLOW mode.
3	DRUM UP	O	Head drum motor rotation speed up signal.
4	SS + DRUM SHIFT	O	Signal for indicating SLOW/STILL modes and alternation of drum motor control data. (3 value voltage)
5	MC - BR	O	Brake signal for capstan motor.
6	C - Vs CUT	O	Cut off for capstan motor control voltage in SLOW / STILL modes.
7	0 / 1 DATA	I	CTL pulse duty detection signal input. Used for VISS detection.
8	-	-	-
9	PAL- L(MESECAM H)	I	Color system indication signal input.
10	FL- START SW	I	Switch input indicating start of cassette loading or discharge by cassette mechanism.
11	-	-	-
12	RESET	I	Initial reset terminal for this IC.
13	CLK 1	-	Clock OSC during power failures.
14	CLK 2	-	Frequency is 32.768kHz.
15	VSS	-	Ground terminal
16	CF 1	-	IC clock OSC terminal.
17	CF 2	-	Frequency is 13.31MHz.
18	VDD	-	IC power supply terminal.(5Vdc)
19	T. END S.	I	Sensor signal input for tape end detection.
20	T. TOP S.	I	Sensor signal input for tape beginning detection.
21	POWER DOWN	I	Power failure detection terminal.
22	T. REEL S.	I	Pulse input for detection of take-up reel table rotation.
23	TAPE SPEED	I	Input of result of tape speed discrimination by digital servo IC.
24	AFT - C	I	Tuner AFT S-curve signal input for tuner AFT control.
25	ENV.	I	Video head envelope detection signal input for ATR function.
26	HIFI ENV.	I	Hi-Fi audio head envelope detection signal input for ATR function. (Hi-Fi model only)
27	SHORT TEST	I	REC mode indication signal input (REC 5V).
28	W. ASP/ AV CTL IN	I	AV source selection signal input from AV terminal.
29	A DUB	O	Signal for indicating audio dubbing mode.
30	STILL + SLOW	O	STILL or SLOW modes indication signal output.
31	C - FG P.	I	FG signal input of capstan motor.
32	-	-	-
33	CTL P.	I	CTL head recording / playback pulse signal input.
34	H SYNC	I	Sync. signal input for existing channel discrimination and TV system discrimination.
35	RF SW P.	I	RF switching pulse input, created by head drum PG.
36	REMOCON	I	Remote control signal input.
37	AFT MUTE	O	"H" output during TU AFT mute. (V-syn model only)
38	G9	O	Display grid outputs (FLD).
39	G8	O	
40	G7	O	
41	G6	O	
42	G5	O	
43	G4	O	
44	G3	O	
45	G2	O	
46	G1	O	
47	VDD	-	IC power supply input.(5Vdc)
48	V LOAD	O	-23V input for FLD drive.
49	SEG i	O	Display segment outputs (FLD). (Includes key-scan output)
50	SEG k	O	
51	SEG j	O	
52	SEG i	O	
53	SEG h	O	
54	SEG g	O	

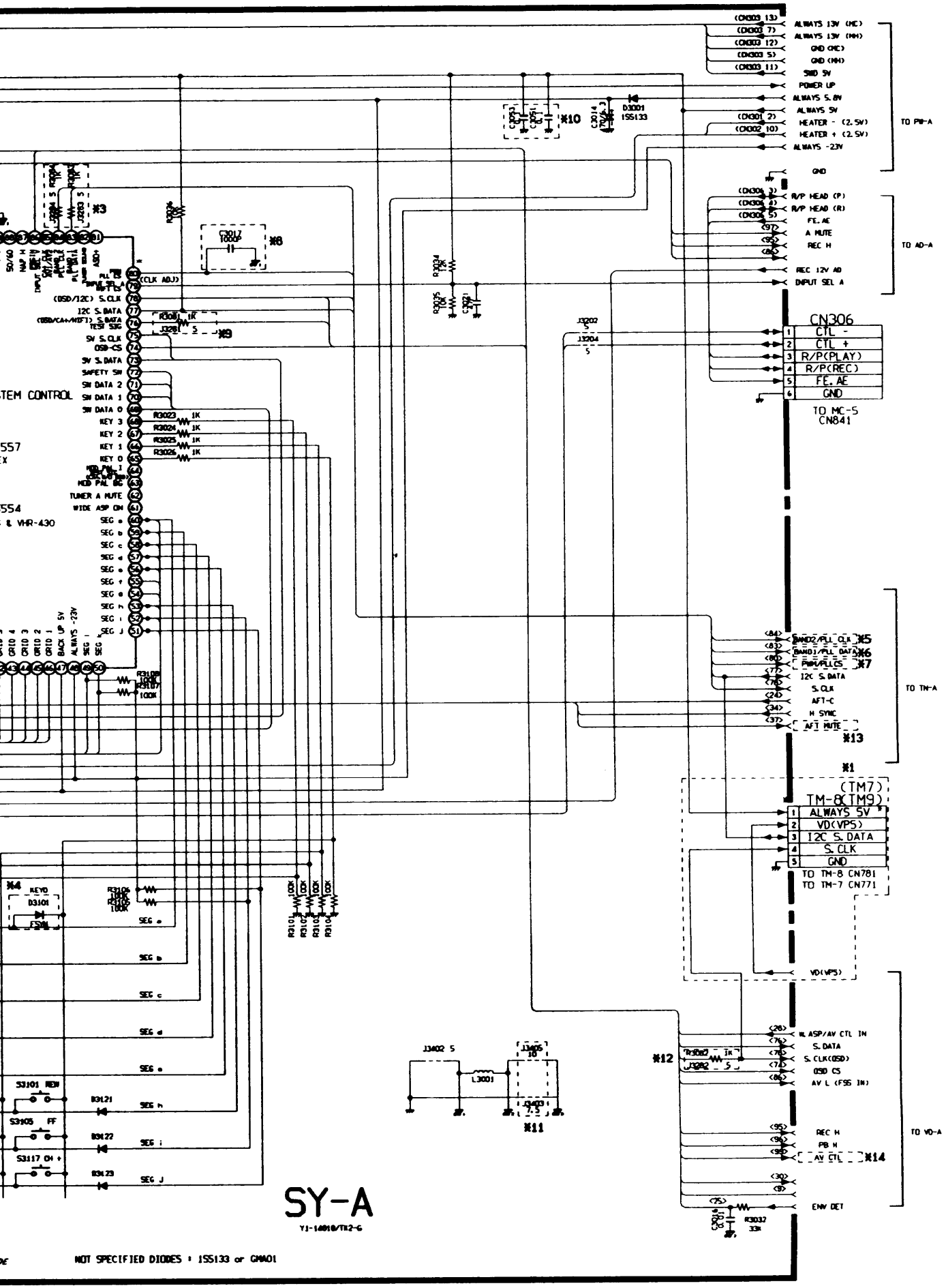
No.	Name	I/O	I/O Signal Function
55	SEG f	O	Display segment outputs (FLD). (Includes key-scan output)
56	SEG e	O	
57	SEG d	O	
58	SEG c	O	
59	SEG b	O	
60	SEG a	O	
61	WIDE ASP ON	O	Signal for wide aspect TV-system indication.
62	TUNER A MUTE	O	Signal for disable tuner-audio output.
63	RF PAL BG	O	Signal for RF output TV-system setting (PAL - BG).
64	RF PAL I	O	Signal for RF output TV-system setting (PAL - I).
65	KEY IN 0	I	Operation key data inputs.
66	KEY IN 1	I	
67	KEY IN 2	I	
68	KEY IN 3	I	
69	SW DATA 0	I	3-bit data indicating operation position of mechanism.
70	SW DATA 1	I	
71	SW DATA 2	I	
72	SAFETY SW	I	Terminal for accidental erasure prevention switch. No operation to record mode while "HIGH" is input.
73	SV S. DATA	O	Output 8-bit X 4 serial data giving operation mode and tracking data,etc., to digital servo IC.
74	OSD CS	O	Chip enable (access) signal output to OSD IC.
75	SV S. CLK	O	The clock pulse for digital servo IC.
76	S. DATA (OSD / CH+ / Hi-Fi)	I/O	Terminal for communication of respective data with OSD IC, CH+ control IC, and Hi-Fi audio IC.
77	I2C S.DATA	I/O	Data exchange with tuning memory IC and VPS IC.
78	S. CLK (OSD/I2C)	O	The clock pulse for OSD IC and tuning memory IC.
79	INPUT SEL A	O	Signal for selecting audio input source.
	HIFI CS	O	Chip enable (access) signal to Hi-Fi audio IC.
80	PLL CS	O	Chip enable signal output to tuner PLL tuning system IC. (F-syn model)
	TU PWM	O	Tuning voltage output (PWM signal). (V-syn model)
81	-	-	-
82	TU SOUND (I/BG)	O	TV system indication signal output (PAL I or BG).
83	BAND 1	O	Tuning band data(BAND 1 and 2 ; for V-syn model).
	PLL DATA	O	Data exchange with tuner PLL IC (for F-syn model)
84	BAND 2	O	BAND 1 and 2 ; (L,L)=VHF-LOW (L,H)=VHF-HIGH (H,L)=UHF (H,H)=SKIP. (for V-syn model)
	PLL CLK	O	The clock for PLL IC of tuner unit (for F-syn model)
85	CH+ CLK	O	The clock for CH+ input/output source selection IC.
	AV1 / AV2	O	Signal for selecting AV-input (video/audio) source.
86	INPUT SEL V	O	Signal for selecting video input source.
	FSS IN	I	CH+ mode control signal input (CH+ model).
87	NAP H	O	" H " output during NTSC (NAP) playback mode.
88	50 / 60	O	" LOW " output during NTSC (NAP) mode. (60 field mode)
89	VSS	-	IC ground terminal.
90	VDD	-	IC power supply input.(5Vdc)
91	ML- S	O	Loading motor rotation speed (low / medium / high) indication signal.
92	ML- D	O	Loading motor rotation direction (FWD / REV) indication signal.
93	-	-	-
94	NORMAL AD REC	O	Signal for indicating normal audio recording.
95	REC H	O	Signal for indicating recording mode.
96	PB H	O	Signal for indicating playback mode.
97	A MUTE	O	"H" output for disable audio output signal.
98	HIFI IN	I	Hi-Fi mode indication signal input from audio IC.
99	AV CTL	O	AV terminal (pin8 of 21pins AV socket) control signal output.
	ANT / VTR	O	Selection the RF source of ANTENNA or VTR.
100	POWER UP	O	"HIGH" output except when power is off. Indicating that power is ON.

TK14HTTS-A



	X1	X2	X3	X4	X5	X6	X7
VHR-274G	TM-7(PDC):NOT USE TM-8(VPS):BUILT IN	L3003	R3083 R3084	USE	PLL CLK	PLL DATA	PLL CS
VHR-274EX	TM-7(PDC):OPTION TM-8(VPS):OPTION	L3003	R3083 R3084	USE	PLL CLK	PLL DATA	PLL CS
VHR-430	TM-7(PDC):NOT USE TM-8(VPS):NOT USE	J3404	J3283 J3284	NOT USE	BAND 2	BAND 1	PWM

	X8	X9	X10	X11	X12	X13	X14
VHR-274G	NOT USE	R3081	USE	J3403	R3082	NOT USE	USE
VHR-274EX	NOT USE	R3081	USE	J3403	R3082	NOT USE	USE
VHR-430	USE	J3281	NOT USE	J3405	J3282	USE	NOT USE


ALWAYS 13V (MC)
ALWAYS 13V (MM)
GND (MC)
GND (MM)
SWD 5V
POWER UP
ALWAYS 5.8V
ALWAYS 5V
HEATER - (2.5V)
HEATER + (2.5V)
ALWAYS -23V
GND
TO PB-A
R/P HEAD (P)
R/P HEAD (R)
FE. AE
A MUTE
REC H
REC 12V AD
INPUT SEL A
TO AD-A
CN306
CTL -
CTL +
R/P(PLAY)
R/P(REC)
FE. AE
GND
TO MC-S
CN841
(CLK ADJ)
(OSD/I2C) S.CLK
I2C S.DATA
SW S.CLK
OSD-CS
SW S.DATA
SAFETY SW
SW DATA 2
SW DATA 1
SW DATA 0
KEY 3
KEY 2
KEY 1
KEY 0
TUNER A MUTE
WIDE ASP ON
SEG a
SEG b
SEG c
SEG d
SEG e
SEG f
SEG g
SEG h
SEG i
SEG j
R3023 1K
R3024 1K
R3025 1K
R3026 1K
R3108 100K
R3107 100K
R3106 100K
R3105 100K
R3104 100K
R3103 100K
R3102 100K
R3101 100K
BAND2/PLL CLK
BAND1/PLL DATA
PWM/PLLCS
I2C S.DATA
S.CLK
AFT-C
H SYNC
AFT MUTE
TO TM-A
(TM7)
TM-8(TM9)
ALWAYS 5V
VD(VPS)
I2C S.DATA
S.CLK
GND
TO TM-8 CN781
TO TM-7 CN771
VD(VPS)
WL ASP/AV CTL IN
S.DATA
S.CLK(OSD)
OSD CS
AV L (FSS IN)
REC H
PB H
AV CTL
ENV DET
TO VD-A
D3001 1SS133
D3101 FSM4
L3001
S3101 REW
S3105 FF
S3117 CH +
SEG a
SEG b
SEG c
SEG d
SEG e
SEG h
SEG i
SEG j
SY-A
YJ-14010/TR2-G
NOT SPECIFIED DIODES : 1SS133 or GMA01